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TECHNOLOGY CENTER 2800

December 18, 2001

TO: Commissioner for Patents  
Attn: Eric W. Thomas  
Patent Examining Corps  
Facsimile Center  
Washington, D.C. 20231

FROM: Mark Muller

OUR REF: 884.240US1

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\* Please deliver to Examiner Eric W. Thomas in Art Unit 2831. \*

Document(s) Transmitted: Amendment and Response Under 37 C.F.R. 1.116 (11 pgs); Clean Version of Pending Claims (6 pgs)

Total pages of this transmission, including cover letter: 18 pgs

If you do NOT receive all of the pages described above, please telephone us at 612-373-6900, or fax us at 612-339-3061.

In re. Patent Application of: Larry Eugene Mosley

Serial No.: 09/537,274

Filed: March 29, 2000

Title: MULTI-LAYER CHIP CAPACITOR

Examiner: Eric W. Thomas

Group Art Unit: 2831

Docket No.: 884.240US1

Please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

By: Ann M. McCrackin  
Name: Ann M. McCrackin  
Reg. No.: Reg. No. 42,858

I hereby certify that this paper is being transmitted by facsimile to the U.S. Patent and Trademark Office on the date shown below.

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EXPEDITED PROCEDURE - EXAMINING GROUP 2831

S/N 09/537,274

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Larry Eugene Mosley

Examiner: Eric W. Thomas

Serial No.: 09/537,274

Group Art Unit: 2831

Filed: March 29, 2000

Docket: 884.240US1

Title: MULTI-LAYER CHIP CAPACITOR

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12-20-01

AMENDMENT & RESPONSE UNDER 37 C.F.R. § 1.116

Box AF  
Commissioner for Patents  
Washington, D.C. 20231

In response to the final Office Action mailed November 7, 2001, please amend the application as follows:

IN THE CLAIMS

Please substitute the claim set in the appendix entitled Clean Version of Pending Claims for the previously pending claim set. The substitute claim set is intended to reflect amendment of previously pending claims 1, 2, 9, 11, 14, 15, and 19. The specific amendments to individual claims are detailed in the following marked up set of claims.

1. (Twice Amended) A multi layer integrated circuit capacitor comprising:
  - a substrate;
  - a first conductive layer located over and contacting the substrate;
  - a first insulator layer located over and contacting the first conductive layer, the first insulator layer not contacting the substrate;
  - a second conductive layer located over the first insulator layer;
  - a second insulator layer located over the second conductive layer;
  - a third conductive layer located over the second insulator layer;
  - a third insulator layer located over the third conductor layer; and
  - a plurality of conductive vias downwardly extending through the third insulator layer to provide electrical interconnection to the first, second and third conductor layers.